FIGURE 1
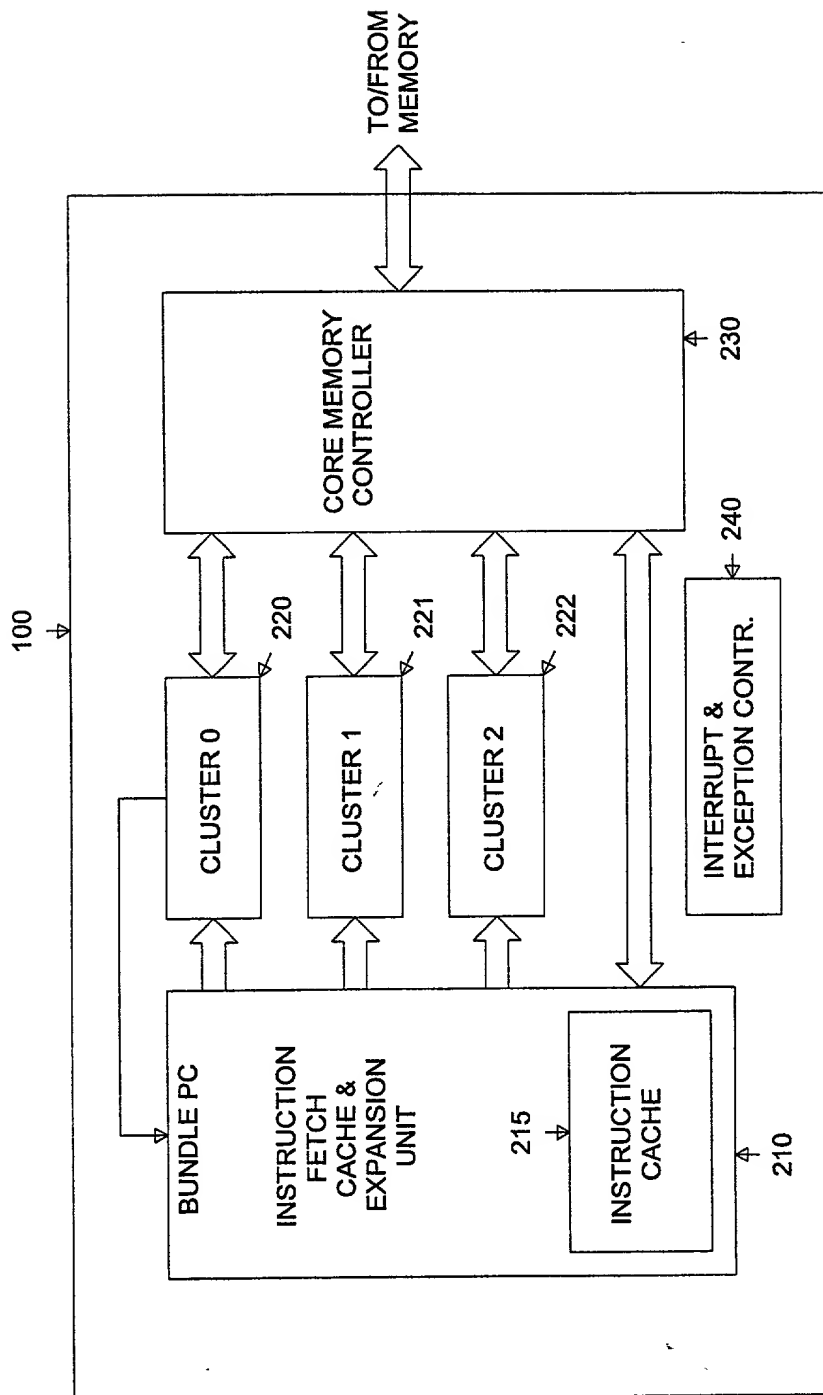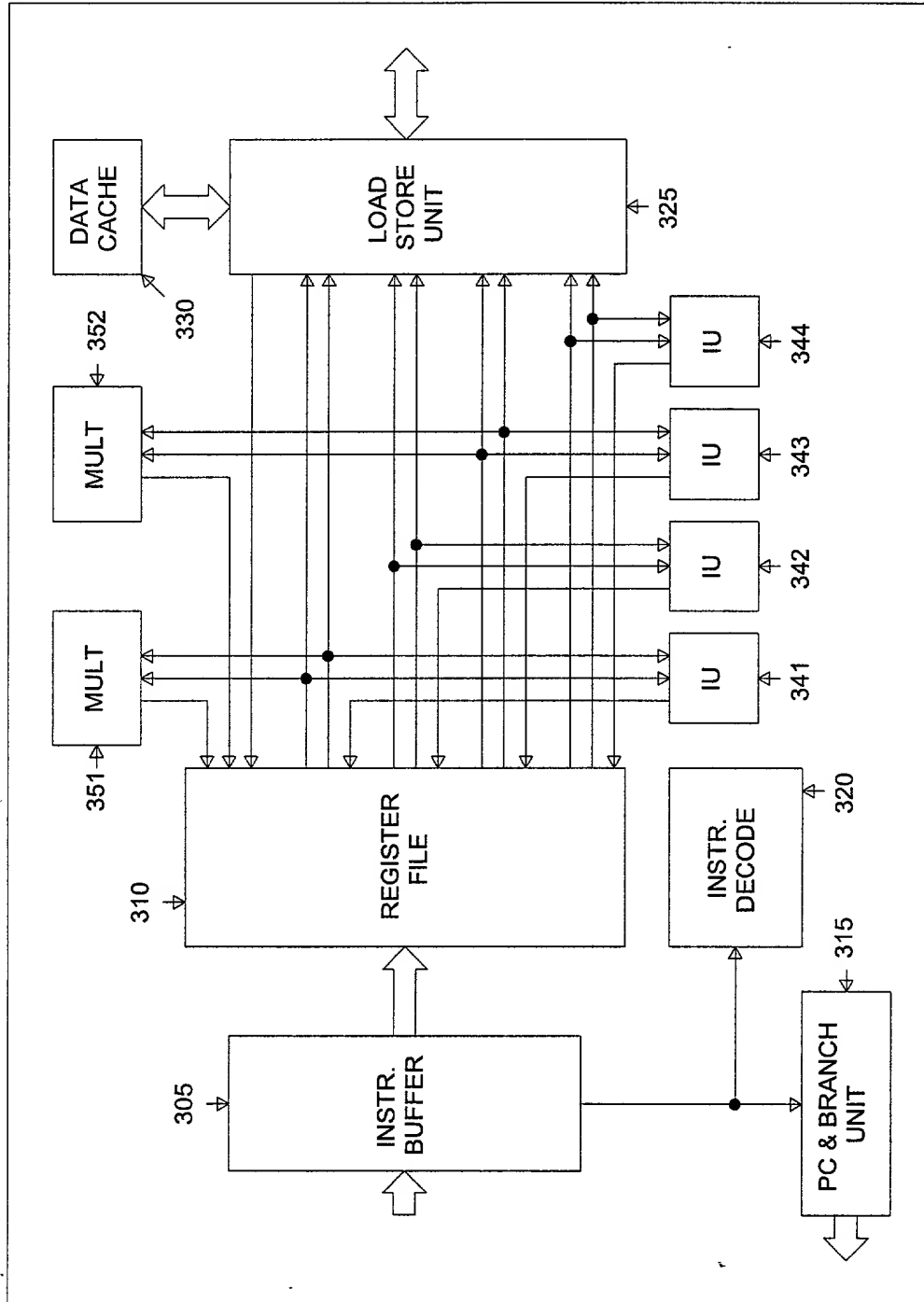
FIGURE 2

FIGURE 3
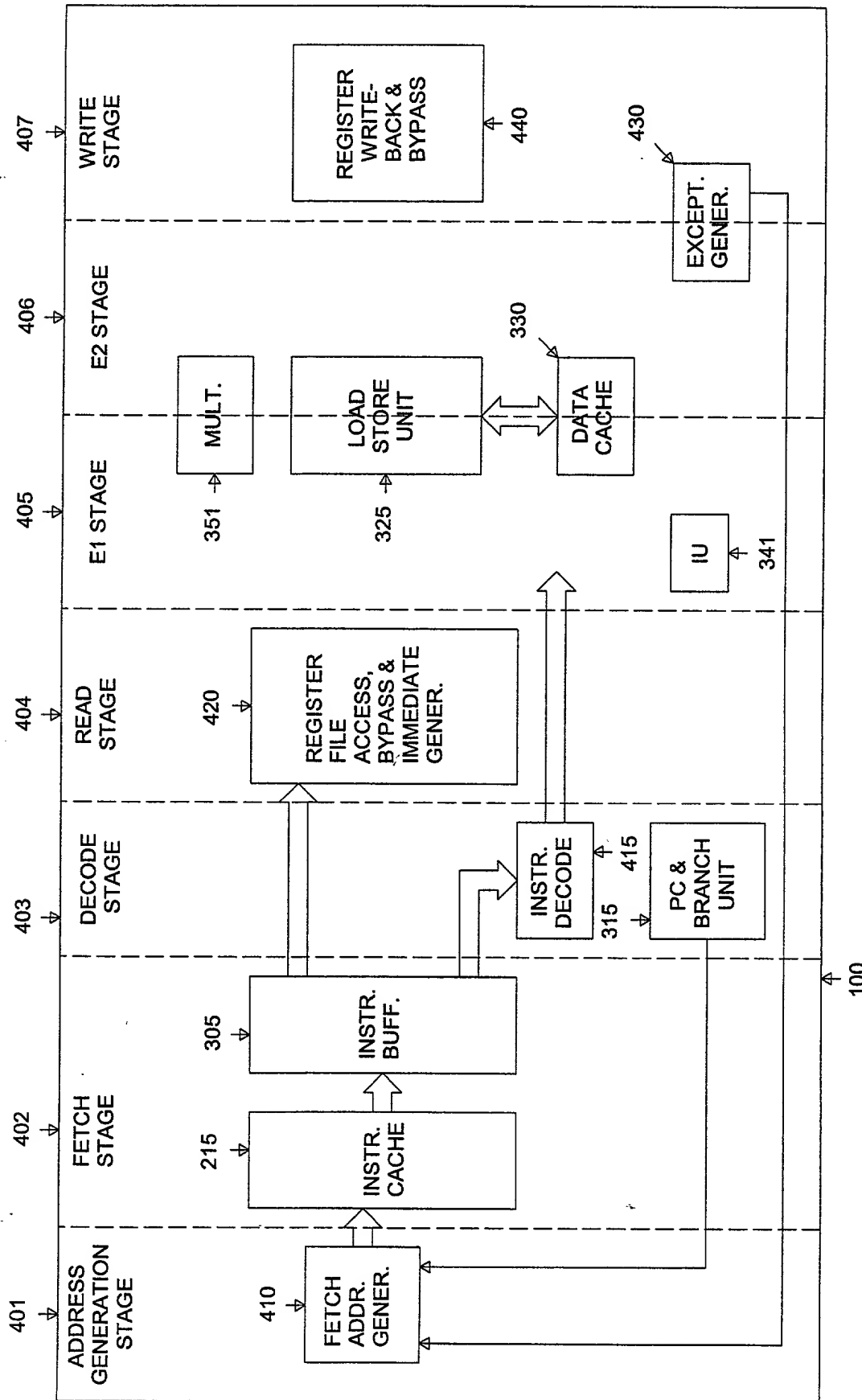
FIGURE 4
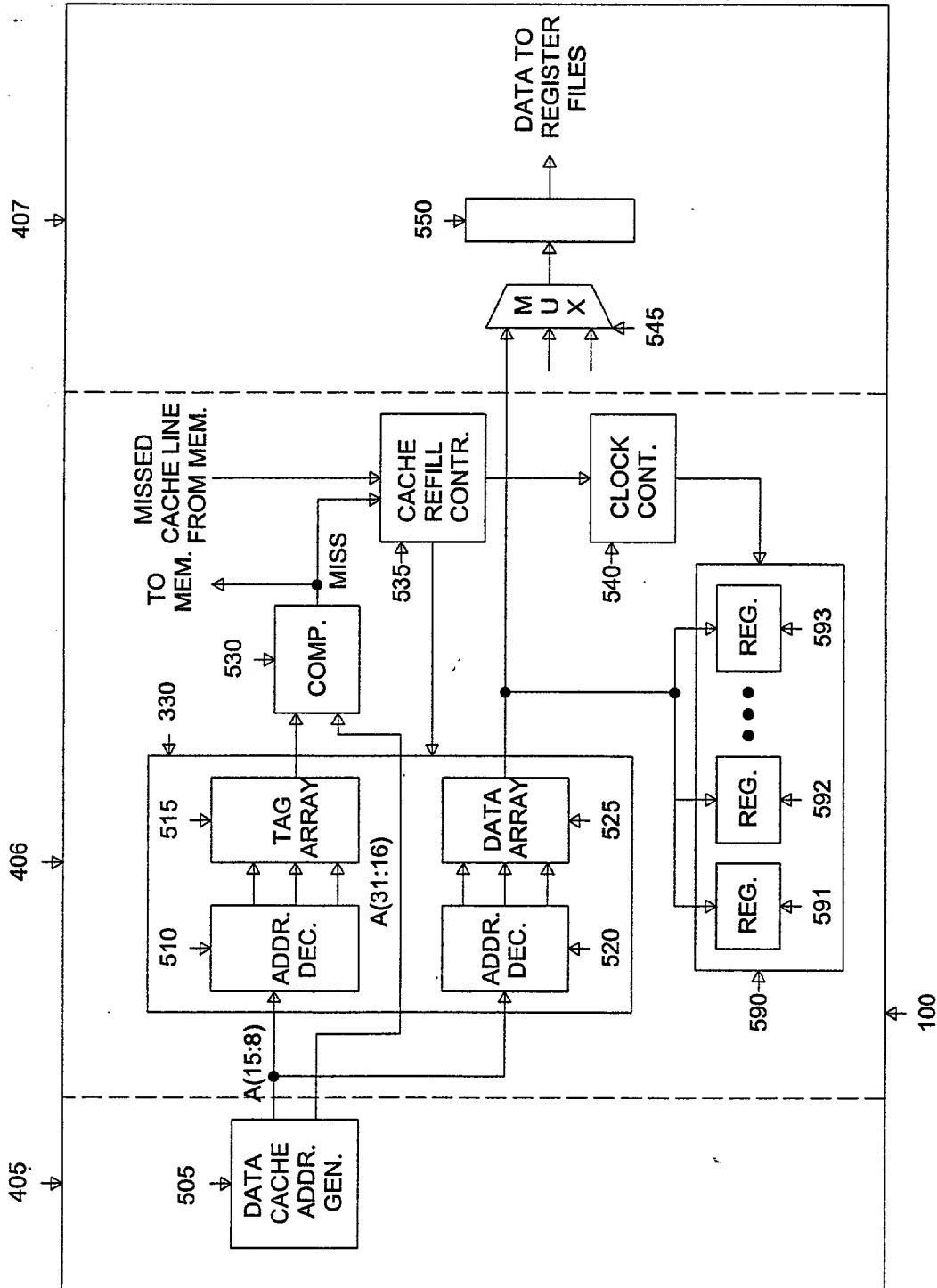
FIGURE 5

START

100

CACHE ADDRESS IS DECODED AND APPLIED
TO TAG ARRAY 515 AND DATA ARRAY 525 ← 605

CACHE DATA IS SENT VIA BYPASS CIRCUITRY 590
TO REGISTERS 591-593 IN OTHER PIPELINE STAGES ← 610

COMPARATOR 530 GENERATES CACHE MISS SIGNAL ← 615

CLOCK CONT. 540 HALTS CLOCKS AND STALLS PIPELINE ← 620

CACHE REFILL CONTROLLER 353 LOADS MISSED CACHE
LINE INTO DATA CACHE 330 AND READS DATA FROM ← 625
MISSED ADDRESS IN RELOADED CACHE LINE

CLOCK CONTROLLER 540 GENERATES EARLY CLOCK
SIGNAL THAT LOADS MISSED CACHE DATA VIA ← 630
BYPASS CIRCUITRY 590 INTO REGISTERS 591-593

CLOCK CONTROLLER 540 RESTARTS CLOCKS AND ← 635
ENDS PIPELINE STALL

END

600

FIGURE 6